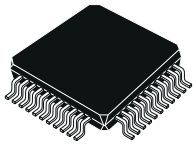
STLC30R80

INTEGRATED RINGING SLIC FOR SHORT LOOP APPLICATIONS

- MONOCHIP SLIC SUITABLE FOR SHORT LOOP APPLICATIONS
- IMPLEMENTES ALL KEY FEATURES OF THE BORSHT FUNCTION
- INTEGRATED RINGING
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME
- ON HOOK TRANSMISSION
- LOW POWER DISSIPATION IN ALL OPERATING MODES
- AUTOMATIC DUAL BATTERY OPERATION
- INTEGRATED RING TRIP DETECTION
- METERING PULSE INJECTION
- LOOP START, GROUND START FEATURES
- SURFACE MOUNT PACKAGE
- -40 TO +85°C OPERATING RANGE



TQFP44 (10 x 10)

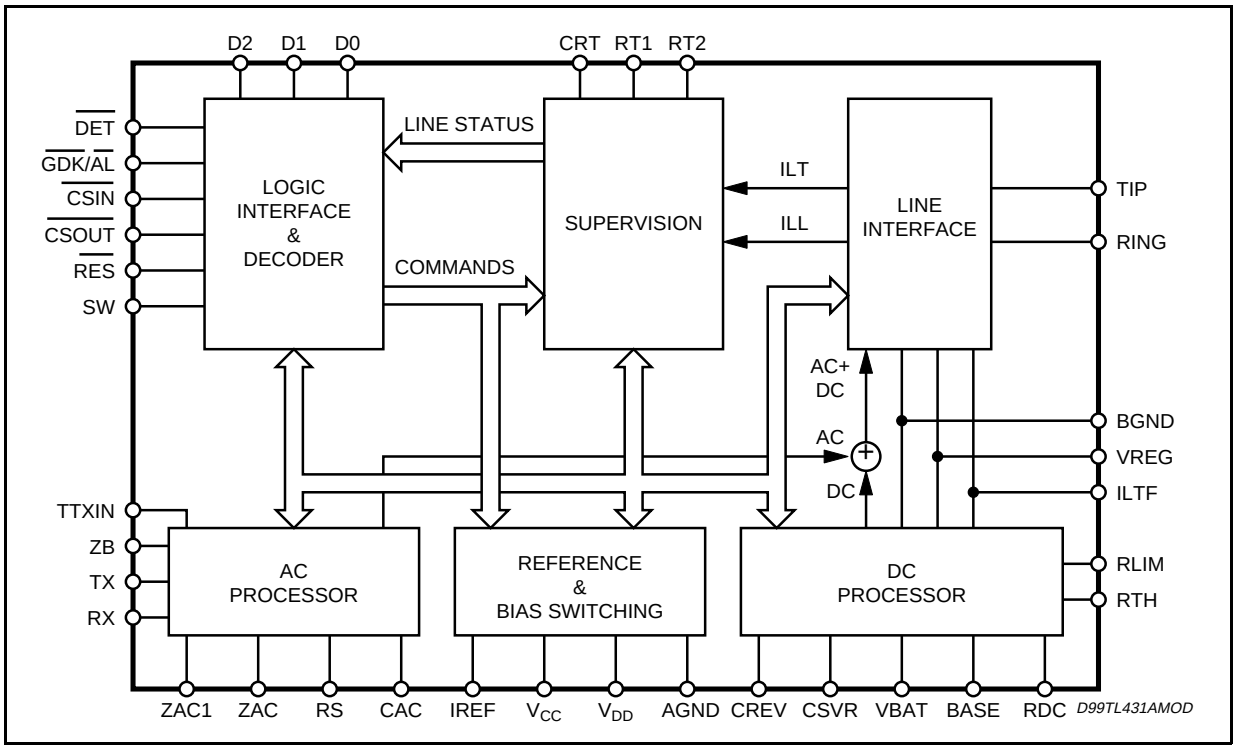
ORDERING NUMBER: STLC30R80

DESCRIPTION

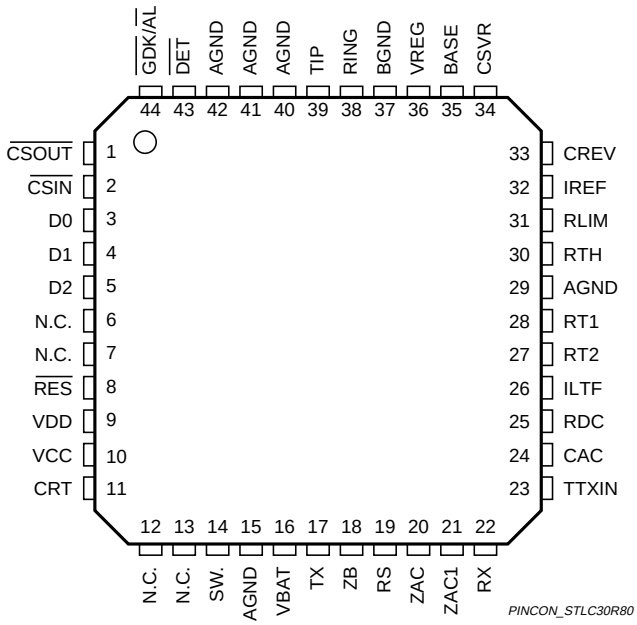
The STLC30R80 is a SLIC device suitable for short loop applications. The SLIC provides the generation of the ringing signal and the standard battery feeding with full programmability of the DC characteristic.

In particular two external resistors allow to set the limiting current value (up to 50mA) and the value of the resistive feeding when not in constant current region.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{BAT}	Battery voltage	-80 + V_{CC} to +0.4 -80 + V_{REL} to + 0.4	V V
V_{CC}	Positive supply voltage	-0.4 to +7	V
V_{DD}	Control Interface Supply Voltage	-0.4 to +7	V
A/R/BGND	AGND respect BGND	-2 to +2	V

OPERATING RANGE

Symbol	Parameter	Value	Unit
T_{opT}	Operating temperature range	-40 to +85	°C
V_{CC}	Positive supply voltage	4.75 to 5.25	V
V_{DD}	Control Interface Supply Voltage	3 to 5.25	V
V_{BAT}	Battery voltage	-72 to -15	V
A/BGND	AGND respect BGND	-0.3 to +0.3	V
PD (70)	Max. power dissipation @ Tamb = 70°C	1.1	W
PD(85)	Max. power dissipation @ Tamb = 85°C	0.9	W

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient	Typ.	60	°C/W

PIN DESCRIPTION

Pins	Name	Description
1	$\overline{\text{CSOUT}}$	Chip-Select for output control bits $\overline{\text{DET}}$ and $\overline{\text{GDK}}$. Active Low. (*)
2	$\overline{\text{CSIN}}$	Chip-Select for input control bits latches D0 D1 D2 R0 R1 . Active Low. (*)
3	D0	Control Interface input bit 0. (*)
4	D1	Control Interface input bit 1. (*)
5	D2	Control Interface input bit 2. (*)
6	N.C.	Not connected
7	N.C.	Not connected
8	$\overline{\text{RES}}$	Reset Input; active low. After activation the SLIC is put in Power Down state
9	V_{DD}	Control interface Power Supply. V_{DD} = 3.3V or V_{DD} = V_{CC}.
10	V_{CC}	Positive Power Supply (+5V).
11	CRT	Ring-Trip time constant capacitor.
12	N.C.	Not connected
13	N.C.	Not connected
14	SW	Internal switch/limiting current programming pin.
15	AGND	Analog Ground
16	V_{BAT}	Negative Battery Supply.
17	TX	4 wires output stage (Transmitting Port).
18	ZB	Cancelling input of Balance Network for 2 to 4 wires conversion.
19	RS	Protection resistors image. The image resistor is connected between this node and ZAC.
20	ZAC	AC impedance synthesis.
21	ZAC1	RX buffer output/ AC impedance is connected between this node and ZAC.
22	RX	4 wires input stage (Receiving Port). A 100K external resistor must be connected to AGND to bias the input stage.
23	TTXIN	Metering Signal Input (AC) and Line Voltage Drop Programming (DC). If not used must be connectd to AGND.
24	CAC	AC feedback input/ AC-DC split capacitor is connected between this node and ILTF.
25	RDC	DC current feedback input. The RDC resistor is connected between this node and ILTF.
26	ILTF	Transversal Line Current Image.
27	RT2	Input pin to sense ringing current , for Ring-Trip detection.
28	RT1	Input pin to sense ringing current , for Ring-Trip detection.
29	AGND	Analog ground.
30	RTH	Off-Hook threshold programming pin.
31	RLIM	Limiting current programming pin.
32	IREF	Voltage reference output to generate internal reference current.
33	CREV	Reverse polarity transition time programming.
34	CSVR	Battery supply filter capacitor.
35	BASE	Driver of the external transistor. Connected to the base.
36	VREG	Regulated voltage. Provides the negative supply to the power line drivers. It is connected to the emitter of the external transistor.
37	BGND	Battery ground.
38	RING	B wire termination output. IB is the current sunk into this pin.
39	TIP	A wire termination output. IA is the current sourced from this pin.
40	AGND	Analog ground.

CONTROL INTERFACE

INPUTS			OPERATING MODE	OUTPUTS	
D0	D1	D2		$\overline{DET}$ (Active Low)	$\overline{GDK}/\overline{AL}$ (Active Low)
0	0	0	Power down	disable	disable
0	0	1	Stand-by	off/hk	gnd-key
0	1	0	Active N.P.	off/hk	gnd-key
0	1	1	Active R.P.	off/hk	gnd-key
1	0	0/1	Ringing	ring/trip	disable
1	1	1	High Impedance Feeding	off/hk	disable
1	1	0	Ground Start	off/hk	gnd-key

A parallel interface allow to control the operation of STLC30R80 through a control bus:

- D0 D1 D2 latched input bits defining the Slic operation mode
- $\overline{DET}$ and $\overline{GDK/AL}$, tri-state outputs, signal the status of the loop: On/Off-Hook and Ground-Key. Pin $\overline{GDK/AL}$ goes low also when the device thermal protection is activated or a line fault (Tip to Ring, Tip and/or Ring to Ground or VBAT) is detected (flowing current ≥ 7.5mA).
- $\overline{CSIN}$: chip select for input bits, active Low, strobes the data present on the control bus into the internal latch.
- $\overline{CSOUT}$: chip select for output bits ; active Low , when high $\overline{DET}$ and $\overline{GDK/AL}$ goes tri-state.

D0 D1 D2 $\overline{CSIN}$ and $\overline{CSOUT}$ inputs are provided with a 15µA pull-down current to prevent uncontrolled conditions in case the control bus goes floating.

According to the table 6 operating modes can be set:

1) Power-Down.
2) Stand-By.
3) Active N.P.
4) Active R.P.
5) Ringing
6) High Impedance Feeding.

Power-Down

It's an idle state characterised by a very low power consumption; any functionality is disabled. It can be set during out of service periods just to reduce the power consumption.

It is worth noticing that two other conditions can set the Slic in idle state but with some differences as reported in the table:

Idle State	$\overline{DET}$	$\overline{GDK}/\overline{AL}$
Power Down	Disable	Disable
Reset	Disable	Disable
Thermal Alarm	Low	Low

Stand-By.

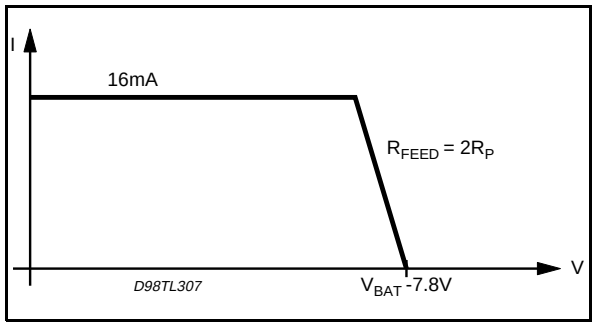
Mode selected in On-Hook condition when high immunity to common mode currents is needed for the $\overline{DET}$ bit.

To reduce the current consumption, AC feedback loop is disabled and only $\overline{DET}$ and $\overline{GDK/AL}$ detectors are active.

DC current is limited at 16mA (not programmable); feeding characteristic shown in fig. a.

The voltage drop in on-hook condition is 7.8V.

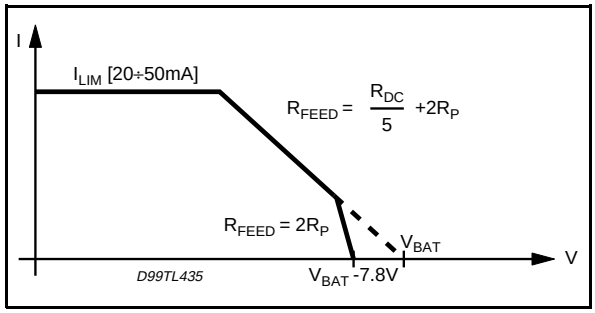
Figure a: STLC30R80 DC Characteristic in Stand-By Mode.



Active

Mode selected to allow voice signal transmission. When in ACTIVE mode the voltage drop in on-hook condition is 7.8V in order to allow proper on-hook transmission (Fig. b).
Resistive Region is programmable by means of external resistor R_{DC}, limiting current can be selected by R_{LIM} and R_{switch} resistor.

Figure b. STLC30R80 DC Characteristic in Active Mode.

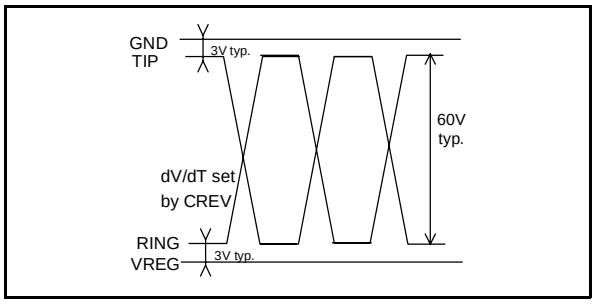


Concerning AC characteristic the STLC30R80 allows to set 2W termination impedance by means of one external scaled impedance that may be complex. Two to four wire conversion is provided by an external network. Such network can be avoided in case of application with COMBOII, in this case the two to four wire conversion is implemented inside the COMBOII by means of the programmable Hybal filter.
When in ACTIVE mode it is also possible to perform battery reversal in soft mode (with programmable transition time) without affecting the AC signal transmission.

Ringing

When ringing mode is selected, by toggling the D2 pin is possible to insert the ringing signal on the line: the ringing frequency is equal to the one applied to the D2 pin. The ringing signal is a balanced trapezoidal wave form where the TIP and RING voltages switch continuously between GND and VREG: VREG is obtained directly from VB1 (VREG = VB1 - 1.8V). The slope of the trapezoidal wave form is set by the external Crev capacitor and it allows to obtain ringing signal with distortion less than 10%: with a fine tuning of this capacitor is possible to obtain distortion value less than 5% (crest factor from 1.25 to 1.35).

Figure c. Typical ringing wave form.



The VB1 value must be higher enough (~70V) in order to obtain ringing signals with more than 40Vrms. The VB2 battery is used only when the line is in off hook and its value can be reduced (typ. 24V) in order to minimize the power consumption.

The ring trip detection is performed sensing the variation of the AC line impedance from on-hook (relatively high) to off-hook (relatively low). This particularly ring trip method allows to operate without DC off-set superimposed on the ringing signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery.

It should be noted that such a meted is optimized for operation on short loop applications and may not operate properly in presence of long loop (>500 Ohm).

As the ring trip is detected the logic indicator $\overline{DET}$ is set low and the ringing is automatically disconnected without waiting for the card controller command (auto ring trip).

Ringing with high REN number

When ringing high number of REN, for example 5REN, or short loops, it could happen that the line AC current, trigger the ring trip circuit producing false ring trip.

If this happens, a proper SW resistor (Rswitch) can be inserted between RLIM and the pin.

The effect of this resistor is to improve the AC current capability in Ring mode avoiding false ring trip in presence of high REN numbers (typ. 5REN) and short loop.

One side effect of Rswitch is to reduce ring trip sensitivity in presence of long loops; therefore it is recommended to adjust Rswitch properly checking the correct behaviour of the device in the two worst-case conditions:

- 0Ω loop, Max REN#
- Max loop length, 1 REN

The lower is the Rswitch value; the higher is the immunity to false Ring trip, producing as side effect a lower Ring trip sensitivity on long loops.

The typical value of Rswitch is shown in the External Components Table (pag.7.13)

High Impedance Feeding.

As Stand-By, this mode is set in On-Hook condition, with further reduced power consumption.

Higher power efficiency turns back a lower immunity of the Off-Hook detector to line common mode currents. The DC feeding shows a constant current characteristic (I_{lim} = 17mA) followed by a resistive range with an equivalent series resistance R_{FEED} = 1600Ω + 2Rp.
Thermal protection circuit is still active, preventing the junction temperature, in case of fault condition, to exceed 150°C

In High Impedance Feeding most of the circuit is switched off, only the circuit, dedicated to Off-Hook detection, is powered. This allows to reduce

Figure d. STLC30R80 DC Characteristic in High Impedance Feeding

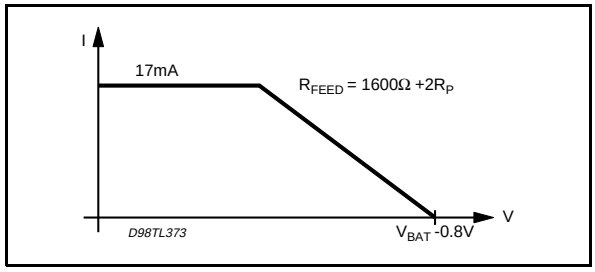
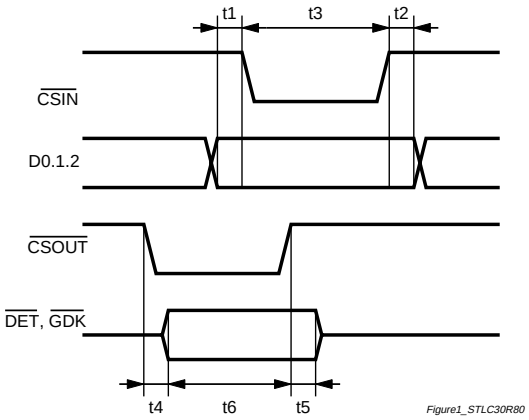


Figure 1. Logic Interface Input Timing

	Min.
t1	100ns
t2	100ns
t3	500ns
t4	100ns
t5	100ns
t6	500ns

Note: All measurements are performed with 100pF on outputs pin and with TTL compatible voltage levels.



the total power consumption in On-hook to 30mW (typical).
The Off-Hook detection threshold is not programmable but defined at a fixed $IDET_{HI}$ = 8mA(max.)

Ground Start.

This mode is selected when the SLIC is adopted in a system using the Ground Start feature. In this mode the TIP termination is set in High Impedance (100kΩ) while the RING one is active and fixed at Vbat +4.8V. In the case of connection of RING termination to GND the sinked current is limited to 30mA. When RING is connected to GND both Off-Hook and Ground-Key detectors become active. Power dissipation in this mode with a -48V battery voltage is 100mW.

PROTECTION CIRCUIT

Suggested protection circuit is based on programmable Trisils (like LCP1511/2) as shown in Fig.2 and Fig. 3, and the surge current is limited by the resistors RPT2 and RPR2, which are PTC types , protecting the device against both lightning and power-cross.

METERING PULSE INJECTION

STLC30R80 provides external pins and components for Metering Pulse injection. TTXIN pin is the input for the 12kHz or 16kHz Metering Pulse injection. This pin also provides a DC constant current source that is injected into the external RDA resistor (typ. 10kΩ) connected between TTXIN pin and AGND. The voltage drop across TIP and RING line amplifiers and, consequentally the AC swing available.

When Metering Pulse injection is not used and voltage drop is not required, TTXIN must be shorted to AGND and RTTX, RDA and CTTX external components must be removed. The TTX cancellation is obtained through an external RTTX and CTTX network connected between TTXIN and CAC pins**.**

MISCELLANEOUS

- Thermal overload: the integrated thermal protection is activated when Tj reaches 150°C typ.; the Slic is forced in Power-down mode, DET and AL are set Low.
- One low cost external transistor allows to reduce the power dissipated in the SLIC itself allowing the use of extreme small size package (TQFP44). The external transistor size/package can be selected depending on the max. power requested by the particular application.

EXTERNAL COMPONENTS LIST

To set the SLIC into operation the following parameters have to be defined:

- The DC feeding resistance "Rfeed" defined as the resistance of the traditional feeding system (most common Rfeed values are: 400, 800, 1000 ohm).
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600 ohm) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The reverse polarity transition time defined as "$\Delta V_{TR}/\Delta T$".
- The constant current limit value "I_{lim}".
- Rth: sets the OFF/Hook DETection threshold

Once, the above parameters are defined, it is possible to calculate all the external components using the following table.

EXTERNAL COMPONENTS

Name	Function	Formula	Typical Value
R_{REF} (*)	Internal current reference programming resistor	$I_{REF} = \frac{1.16}{R_{REF}}$	30.1kΩ ± 1%
C_{SVR}	Battery ripple rejection capacitance	$C_{SVR} = \frac{1}{2\pi \cdot fp \cdot 1.3M\Omega}$	100nF ±10% 100V @ fp = 1.22Hz
C_{RT}	Ring Trip capacitance	$C_{RT} = (25/fring) \cdot 470nF$	470nF ±20% 6V @ 25Hz
R_{DC}	DC sinthesized resistance programming resistor	$R_{DC} = 5[R_{feed} - 2Rp]$ $R_{DC} \geq 1k\Omega$	1.5kΩ ±1%
C_{AC}	AC/DC splitter capacitance	$C_{AC} = \frac{1}{2\pi \cdot fsp \cdot R_{DC}}$	10µF ±20% 15V @ fsp = 10Hz
R_S	Protection resistor image	$R_S = 25 \cdot 2Rp$	2.5kΩ ±1%
ZAC	2 wire AC impedance	$Z_{AC} = 25[Zs - 2Rp]$	12.5kΩ ±1%
ZA	SLIC impedance balancing network	$ZA = 25 \cdot Zs$	15kΩ ±1%
ZB	Line impedance balancing network	$ZB = 25 \cdot Zl$	15kΩ ±1%
C_{COMP}	AC feedback compensation capacitance	$C_{COMP} = \frac{2}{2\pi \cdot fo[100 \cdot Rp]}$	220pF ±20% @ fo = 250kHz
RS1	Sensing resistor for Ring Trip	$1000 \cdot RR$	600kΩ ±0.5%
RS2	Sensing resistor for Ring Trip	$1000 \cdot RR$	600kΩ ±0.5%
Q_{EXT}	External transistor	(1)	BD140, MJD32
RPT1	Line series resistor	≥20Ω	20W 1/4W
RPR1	Line series resistor	≥20Ω	20Ω 1/4W ±1%
R_{LIM} (*)	Current limiting setting resistor	$R_{LIM} = 10^3 \cdot \frac{1.16}{I_{LIM}}$; 26kΩ ÷ 64.9kΩ	51.1kΩ ±1%
R_{SWITCH} (***)	Current limiting setting resistor	$R_{switch}\,[k\Omega] = \frac{24.4k\Omega \cdot R_{LIM}\,[k\Omega]}{R_{LIM}\,[k\Omega] - 24.4k\Omega}$	47kΩ
R_{TH} (**)	OFF/HOOK $\overline{\text{DET}}$ection threshold setting resistor.	$R_{TH} = 200 \cdot \frac{1.16}{I_{TH}}$; 23.7kΩ ÷ 86.6kΩ	26.1kΩ ±1%
C_{REV}	Polarity reversal transition time programming	$C_{REV} = \frac{K}{\frac{\Delta V_{TR}}{\Delta T}}$; $K = \frac{1}{3750}$	47nF for 5.67V/ms
RDA	Output Voltage Drop Adjustment	$RDA = \frac{\Delta Drop \cdot 20k\Omega}{9.6 - \Delta Drop}$	10kΩ (ΔDrop = 3.2V) (2)
R_{TTX}	Teletax Cancellation Resistor	$R_{TTX} = 12.5 \cdot [Re\,(ZL_{TTX}) + 2R_P]$	3.75kΩ
C_{TTX}	Teletax Cancellation Capacitor	$C_{TTX} = \frac{1}{(12.5 \cdot I_m\,(ZL_{TTX}) \cdot 2\pi \cdot f_{TTX})}$	
RPT2	Protection resistor	≥ 8Ω	
RPR2	Protection resistor	≥ 8Ω	
D1	Overvoltage protection		1N4448
D2	Dual Battery Operation		1N4448
CH	Trans-Hybrid Loss Frequency Compensation	CH = CCOMP	220pF ±30%
C_{VCC}	Power Supply Filter		100nF ±20%
C_{VB}	Battery Supply Filter		100nF ±20% 100V

Notes:

(1) Transistor characteristics: $h_{FE} \geq 25$, $I_C \geq 100mA$, $V_{CEO} \geq 60V$, $f_T \geq 15MHz$. PDISS depends on application, see Appendix. For SMD application possible alternatives are MJD350 in D-PACK or BCP53 in SOT223

(2) Typical value needed for 2.2Vrms metering pulse level, if no metering RDA = 0Ω.

(*) R_{REF} and RLIM should be connected close to the corresponding pins of STLC30R80. Avoid any digital line or high voltage swing line to pass close to I_{REF} and R_{LIM} pins. Eventually screen these pins with a GND track.

(**) Inside the formula the coefficient 1.16 must be changed to 1.2 if the selected value of I_{Th} is lower than 5mA.

(***) This resistor must be used only in presence of REN number and short loop see description at page 5/13.

Figure 2. Typical application diagram.

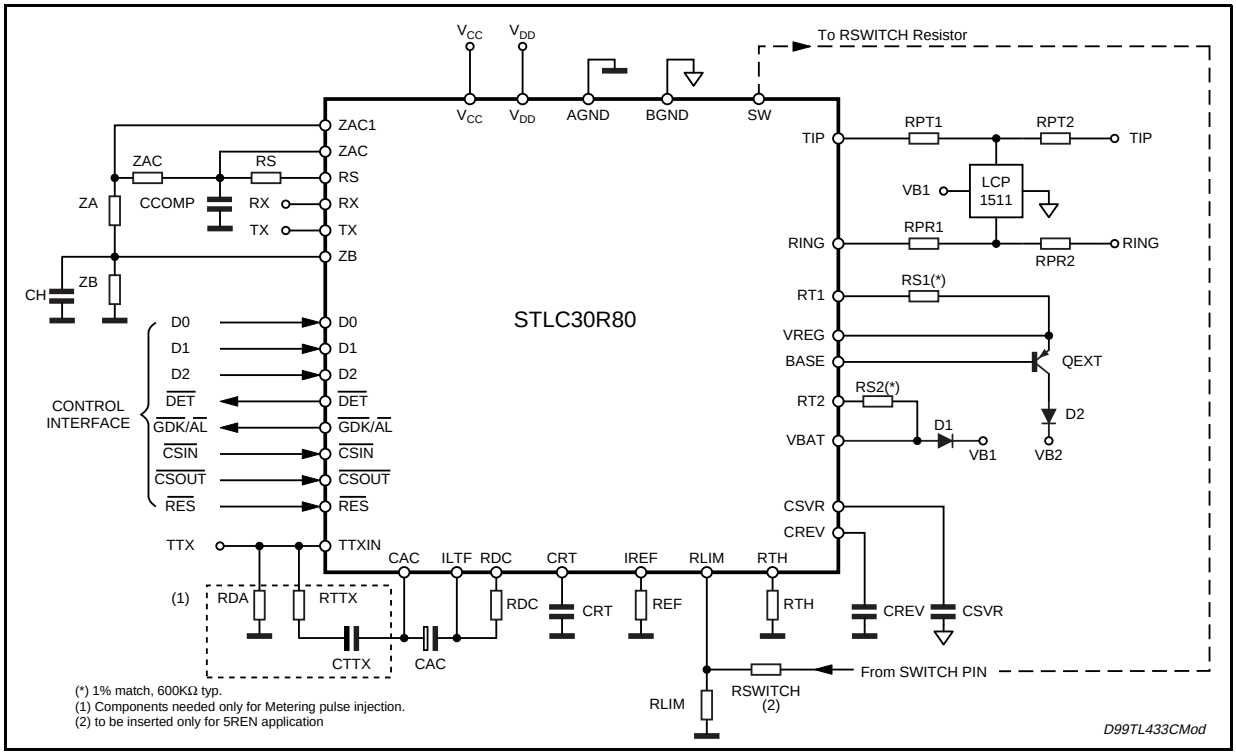
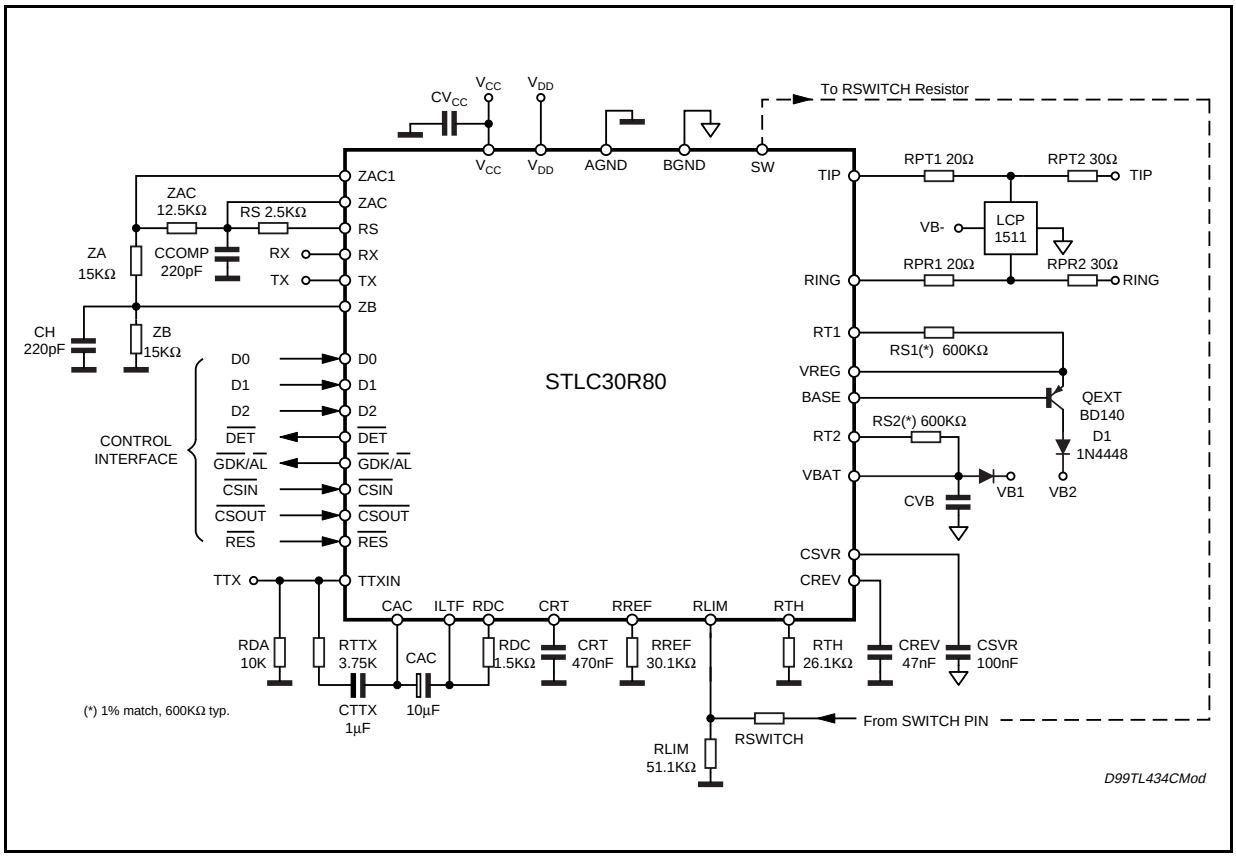


Figure 3. Test Circuit.



ELECTRICAL CHARACTERISTICS (Test Condition, unless otherwise specified: V_{CC} = 5V, V_{DD} = 3.3V, V_{B-} = -48V, AGND = BGND, T_{amb} = 25°C).
Note: the limits below listed are guaranteed with the specified test condition and in the 0 to 70°C temperature range. Performance over -40 to +85°C range are guaranteed by product characterisation.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
AC CHARACTERISTICS							
Zil	Long. Impedance	each wire			40	Ω	
I_{il}	Long. Current Capability AC	H.I. feeding per wire (ON-HOOK)		5		mApk	
		STANDBY or ACTIVE per wire (ON-HOOK)		13		mApk	
		ACTIVE per wire (OFF-HOOK). I_T = Transversal Current		80 -I_T		mApk	
L/T	Long. to transv.	with nominal Rp value	60			dB	C5
T/L	Transv. to long.		40			dB	C3
2wRL	2W return loss.	300 to 3400Hz	22			dB	C6
THL	trans-hybrid loss.	1020Hz; 20Log |VRX/VTX|	30			dB	C2
Ovl	2W overload level	ACTIVE MODE at line terminals on ref. imped.	3.2			dBm	
TXoff	TX output offset		-200		200	mV	
G24	Transmit gain abs.	0dBm 1020Hz	-12.38		-12.02	dB	C4
G42	Receive gain abs.	0dBm 1020Hz	5.74		6.1	dB	C1
G24fq	tx gain variation vs. frequency	rel. 1020Hz, 0dBm 300 to 3400Hz	-0.1		0.1	dB	
G42fq	rx gain variation vs. frequency	rel. 1020Hz, 0dBm 300 to 3400Hz	-0.1		0.1	dB	
V2wp	idle channel noise at line terminals	psophometric		-82	-78	dBmp	C8
V4wp	idle channel noise at TX port	psophometric		-90	-84	dBmp	C7
Thd	total harm. dist. 2w-4w, 4w-2w	0dBm, 1KHz Il = 20 to 45mA			-50	dB	
G_{TTX}	Transfer Gain	V_{TTX} = 100mV_{RMS} @ 16kHz $G_{TTX} = 20\text{Log}\left(\frac{V_L}{V_{TTX}}\right)$ with R_L = 200Ω		14.5		dB	
THD (TTX)	TTX Harmonic Distortion	2.2V_{RMS} = on 200Ω			3	%	
DC CHARACTERISTICS (TTX pin connected to ground)							
Vlohi	Line voltage	Il = 0, H.I. feeding	47	47.4	47.8	V	
Vlo	Line voltage	Il = 0, SBY/ACTIVE/ON-HOOK	38.6	39.9	40.6	V	
Ilims	Short circ. curr.	R_{loop} = 0, SBY	14	16	18	mA	
Ilimb	Short circ. curr.	R_{loop} = 0, H.I. feeding	11	17	20	mA	
Ilima	Lim. current accuracy	Rel to progr. val. 20 to 45mA ACTIVE NP, RP	-10		10	%	
Rfeed	Feed res. accuracy	ACTIVE NP, RP	-10		10	%	
Rfeed H.I.	Feeding resistance	H.I. feeding	1100		2100	Ω	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
Ilact	Feed current ACTIVE	ACTIVE NP, RP Rloop = 1900Ω RDC = 1.5kΩ	18			mA	
Ilsby	Feed current STBY	STY, Rloop = 2.2KΩ RDC = 1.5kΩ	13			mA	
I_{TIP}	Tip Leackage Current	Ground Start			1	µA	
I_{GS}	Ring Lead Current	Ground Sart Ring to GND		33		mA	
I_{DA}	Reference current sourced by TTX IN pin for Voltage Drop programming			-60		µA	
DETECTORS							
I_{det}	Off-hook current threshold ST-BY, ACTIVE	Rel. to progr. val. 7 to 11mA	-10		+10	%	
		Rel. to progr. val. 3 to 6mA	-20		+20	%	
I_{det} H.I.	Off-Hook current threshold	H.I. feeding	5		8	mA	
Hys	Off/On hook hyst.	ST-BY, ACTIVE		15% I_{det}		mA	
Td	Dialling distortion	ACTIVE	-1		+1	ms	
I_{LL}	Ground Key Current threshold $I_{LL} = I_B - I_A$	TIP to RING to GND or RING to GND		7.5		mA	
I_{gst}	Ground Start Detection Threshold	$I_{gst} = 2 \cdot I_{det}$	-10		+10	%	
DIGITAL INTERFACE INPUTS: D0, D1, D2, $\overline{CSIN}$, $\overline{CSOUT}$							
Vih	Input high voltage	V_{DD} = 3.3V	2			V	
Vil	Input low voltage	V_{DD} = 3.3V			0.8	V	
Iih	Input high current				30	µA	
Iil	Input low current				10	µA	
OUTPUTS: $\overline{DET}$, $\overline{GDK}$ /$\overline{AL}$							
Vol	Output low voltage	Iol = 0.75mA; $\overline{CSOUT}$ = LOW			0.5	V	
Voh	Output high voltage	Ioh = 0.1mA; $\overline{CSOUT}$ = LOW	2.4			V	
I_{OZ}	Tri-State Output Current	$\overline{CSOUT}$ = High	-10		+10	µA	
POWER SUPPLY REJECTION							
PSRRC	V_{CC} to 2W port	Vripple = 0.1Vrms 50 to 4000Hz	27			dB	C9
PSRRB	Vbat to 2W port	Vripple = 0.1Vrms 50 to 4000Hz	30			dB	C9
POWER CONSUMPTION							
I_{CC}	V_{CC} supply current	H. I. Feeding On-Hook SBY On Hook ACTIVE On Hook			1.0 3.5 5.0	mA mA mA	
I_{BAT}	V_{BAT} supply current	H. I. Feeding On-Hook SBY On Hook ACTIVE On Hook			0.5 2.5 4.5	mA mA mA	
I_{DD}	V_{DD} Supply Current	Any operating mode		100	320	µA	

APPENDIX A

Battery voltage autoset

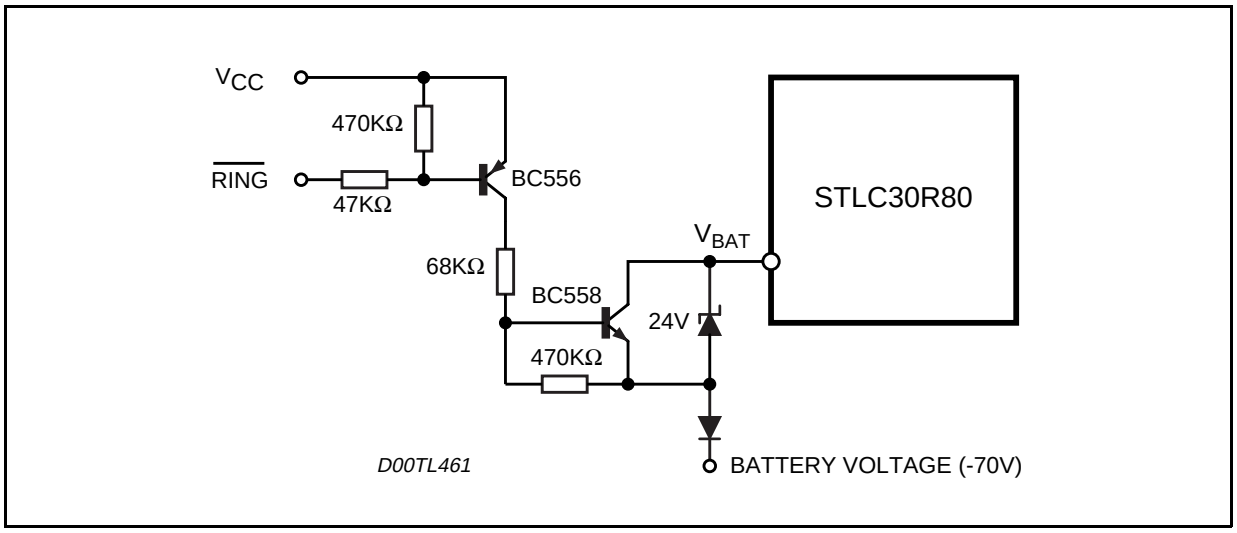
The STLC30R80 shows a line voltage depending on the voltage applied to Vbat pin. In particular in the On-Hook the line voltage is Vbat if the SLIC is put in HI-Z mode or Vbat -7.8V if the SLIC is put in Active mode.

If the battery voltage applied to the Vbat pin is always -70V (necessary to generate the proper ringing signal), during the On-Hook the line voltage is higher than 60V.

A simple circuit to generate the proper Off-Hook battery voltage can be used starting from the -70V as shown in the below figure A1.

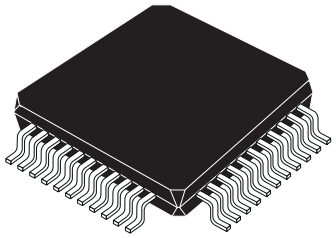
The RING command (active low) is used to switch on the NPN transistor and apply the battery voltage directly to the Vbat pin. When the RING command is high the NPN transistor is off and the zener diode reduces the voltage applied to the Vbat pin.

Figure A1.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10)